ABSTRACT OF THE DISCLOSURE

A memory module for use in a two rank memory module system includes a plurality of memory devices and a control circuit. In one embodiment, the control circuit may be configured to generate a chip select signal that is provided to each of the memory devices. The chip select signal may be dependent upon assertions of a first bank chip select signal and a second bank chip select signal received from a memory controller. The control circuit may be further configured to generate an address signal that is provided to each of the memory devices. The address signal may be asserted dependent upon which of the first bank chip select signal and the second bank chip select signal are asserted.